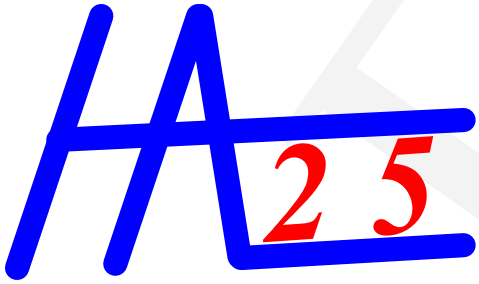

User Manual

HAL25_V2 User Manual v0.2

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Document history

HAL_V2		
Version	Date	Description
0.2 0.1	19/08/2002 12/12/2001	Bias settings updated for positive and negative pulses Based on HAL_V1: • New pad list • VBUF DAC still exist but no more used • IREF pad, specified as test purpose only • Transparent mode: POWER_ENA register state specified
HAL_V1		
Version	Date	Description
0.2	24/10/2001	Physical size schematic updated
0.1	08/06/2001	Draft version before HAL25 returns from foundry

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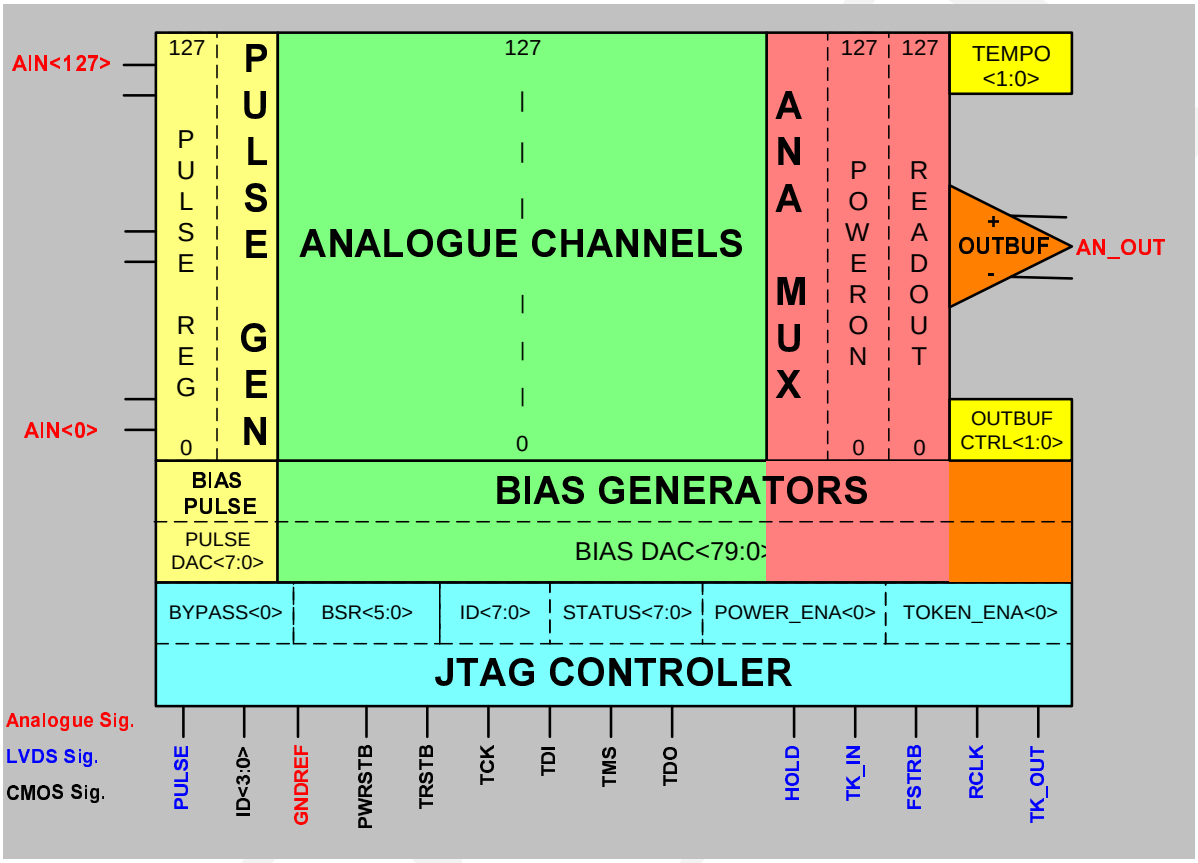
Introduction

HAL25 is an ASIC dedicated to the read-out of silicon strip detectors in the ALICE tracker. The chip contains 128 channels. The read-out of the strips detectors is performed in two steps.

- Parallel Acquisition: Each analogue channels amplifies, shapes within an adjustable time from 1.4 µS to 2.2 µS. Then the signals are sampled in a storage capacitor when HOLD goes high.
- Serial Read-out: An analogue multiplexer transfers the signal from channel<127> down to channel<0> to a differential current output buffer at a 10 MHz rate. A fast clear FRSTB let to abort the readout at any time. Many chips can be daisy-chained.



Rq: Only signals for normal use are shown in the block diagram.

Set-up and test of the circuit are performed with programmable registers accessed via an embedded slow control interface.
The set-up consists mainly to

- Load the DAC which bias the analogue blocks
- Authorise HAL25 to be serially read-out i.e. to let the token used by the logic of the analogue multiplexer to flow through the chip

Different tests are provided to verify the functionality of the circuit

- Pulse Test Mode
- Transparent Test Mode
- Boundary Scan Test Mode

Control Interface

The control interface of HAL25 complies with the JTAG IEEE 1149.1 standard. It allows the access of the registers of the chip especially for the setting of the bias and the selection of the running mode.
On Power on Reset (PWRSTB) or JTAG Reset (TRSTB) an internal reset is generated. The Test Access Port (TAP) of the controller enters in the Test-Logic-Reset state and the BYPASS register is selected.

JTAG Instruction Set

The Instruction Register of the JTAG controller is loaded with the code of the desired operation to perform or with the code of desired internal data register to access.

Instruction	5 Bit Code	Selected Register	Notes
EXTEST	00	BSR	JTAG required instruction
INTEST	03	BSR	JTAG optional instruction
CLAMP	04	BYPASS	JTAG optional instruction
SAMPLE_PRELOAD	05	BSR	JTAG required instruction
BYPASS	1F	BYPASS	JTAG required register
BIAS_DAC	09	BIAS_DAC	
STATUS	0B	STATUS	
PULSE_DAC	0D	PULSE_DAC	
PULSE_REG	11	PULSE_REG	
READ_REG	15	READ_REG	
POWER_ENA	19	POWER_ENAG	
ID_REG	1B	ID_REG	
TOKEN_ENA	1D	TOKEN_ENA	

JTAG Register Set

JTAG registers are implemented with a shift and a shadow register. Only some data registers are designed such a way. Remember that the JTAG standard imposes that the last significant bit of a register is downloaded first.

SEU tolerance and detect

In order to prevent failures due to a Single Event Upset, the most important registers like DAC registers, have been designed with majority vote logic. A detection logic allows the users to know which register has been hit by a SEU.

Register Name	Size	Majority Vote + SEU Detect	Access	Notes
BYPASS	1	N	R Only	
BSR	6	No	R/W	BSR values depend from BSR instructions
BIAS_DAC	72	Yes	R/W	Previous value shifted out during write
PULSE_DAC	8	Yes	R/W	Previous value shifted out during write
PULSE_REG	128	No	R/W	Previous value shifted out during write
READ_REG	260	No	R/W	Previous value shifted out during write
STATUS	8	No	R Only	
POWER_ENA	1	Yes	R/W	Previous value shifted out during write
TOKEN_ENA	1	Yes	R/W	Previous value shifted out during write
ID_REG	8	No	R Only	

Bypass Register

Bypass register consists of a single bit scan register. It is selected after hardware reset, when the TAP is in Test-Logic-Reset state, when its code is loaded in the Instruction Register or when the Instruction Register contains an undefined instruction.

Boundary Scan Register

The Boundary Scan Register, according with the JTAG instructions, test and set the following input and output pads:

Bit #	Corresponding Pad	Type	Signal	Notes
5	LVDS_RDCLKP/N	Input	RDCLK	Readout clock after LVDS conversion
4	LVDS_TK_INP/N – TK_IN_C	Input	TK_IN	Token in, common to LVDS or CMOS inputs
3	LVDS_PULSEP/N	Input	PULSE	Pulse after LVDS conversion
2	LVDS_HOLDP/N	Input	HOLD	Hold after LVDS conversion
1	LVDS_FRSTP/N	Input	FRSTB	Fast Reset after LVDS conversion
0	LVDS_TK_OUTP/N – TK_OUT_C	Output	TK_OUT	Token out, common to LVDS or CMOS outputs

BIAS_DAC register

BIAS_DAC is 72 bits large, it sets simultaneously 9 of the 10 DACs designed in HAL25. As show bellow these 8-bit DACs set the bias voltage and current of the 128 analogue channels, the analogue multiplexer and the analogue output buffer. The internal reference current source can also be adjusted.
After reset the register bits are set to 0, this fixed the minimum power consumption of the analogue channels. The reference current source is set to its nominal value.

Bit #	Name	DAC register
71-64	ISHCON	Shaper Current Bias1
63-56	ISHA	Shaper Current Bias2
55-48	VSHA	Shaper Voltage Bias
47-40	IPRE	PreAmp Current Bias
39-32	VPRE	PreAmp Voltage Bias
31-24	IMUX	Analogue Multiplexer Current Bias
23-16	IBUF	Output Buffer Current Bias
15- 8	VBUF	Output Buffer Voltage Bias (No more used)
7- 0	IREF	Internal Reference Current Source Adjust

PULSE_DAC register

PULSE_DAC register is 8 bits large. It set the current level of the analogue pulse generated by the test pulse logic. After reset the register bits are set to 0.

PULSE_REG register

PULSE_REG register is 128 bits large. It is used during Pulse Test Mode. It selects the channel where the test pulse will be injected. Up to 32 channels among the 128 can be selected. A bit set to 1 enables the corresponding channel. Bits PULSE_REG<127> down to PULSE_REG<0> correspond to analogue channel<127> down to analogue channel< 0>.

READ_REG register

READ_REG register is used to set HAL25 in transparent mode. Transparent mode allows the user to check a single analogue channel among the 128. One can inject a signal in its input and see on a oscilloscope the resulting output signal.
READ_REG is 260 bits large. It gathers 4 daisy-chained sub-registers:

Bit #	Register Name	Size
259-258	TEMPO	2
257-130	READOUT	128
129- 2	POWERON	128
1- 0	OUTBUF_CTRL	2

To select an analogue channel<n> among channel <127> down to channel<0>, 4 bits in the READ_REG have to be set to 1:

- READOUT<n>
- POWERON<n>
- OUTBUF_CTRL<1:0>

Example: To set in transparent mode channel<8>. Code is hexadecimal.

TEMP0 259-260	READOUT 257-130	POWERON 129-2	OUTB. 1-0
3	00000000 00000000 00000000 00000100	00000000 00000000 00000000 00000100	3

STATUS register

This 8-bit register stores the state of the SEU flags of the HAL25 registers. A bit set to 1 indicates that the corresponding register has been hit by a SEU. Registers internal value should not have change because the majority vote logic maintains the right value but it is wise to reload the registers.

Bit #	Bit Name	Corresponding Register
7	FSM	JTAG FSM register
6	IR_REG	JTAG Instruction register
5	POWER_ENA	
4	TOKEN_ENA	
3	PLSCNTRL	
2	PULSEDAC	
1	BIASDAC	
0	OUTBUF_CTRL	

POWER_ENA register

POWER_ENA is a single bit scan register. It enables the power on mechanism of the analogue multiplexer when it is set to 1. This is the default value after a reset thus the multiplexer of HAL25 is ready for a normal readout. Before READ_REG settings it must be fixed to 0.

TOKEN_ENA register

TOKEN_ENA is a single bit scan register. When set to 1, it enables the token signal, TK_IN, used by the analogue mutiplexer to shift through the circuit. After reset, TOKEN_ENA, the token is bypassed, i.e. it flows directly to next HAL25.

ID_REG register

ID_REG is a read only, 8 bit wide, register. The 4 most significant bits are fixed internally. The 4 remaining bits are set via the 4 input pads ID<3:0>.

bit<7>	.	.	.	.	.	.	bit<0>
1	0	1	0	ID<3>	ID<2>	ID<1>	ID<0>

Running HAL25

After power on reset (PWRSTB), or reset (TRSTB):

- All data registers are set to their default value, mainly 0
- JTAG state machine in Test-Logic-Reset state
- JTAG BYPASS register is selected
- Token signal for readout is bypassed

Then the bias registers and an operating mode have to be loaded.

Biasing HAL25

BIAS_DAC register has to be loaded before operating HAL25.
The following table gives the hexadecimal codes, for nominal settings, to down load in BIAS_DAC.

Name	Code Hexa	Value	Dac Resol	Dac Range	Out Range	Notes
ISHCON	A0	-160 nA	1 nA	0 - 255	0 - -255 nA	Shaping time 1.4µs
	32	-50 nA				Shaping time 2.2µs
ISHA	89	+55 µA	400 nA	0 - 255	0 - 100 µA	Shaping time 1.4µs
	32	+20 µA				Shaping time 2.2µs
VSHA	3C	+0.6 V	10 mV	0 - 200	0 - 2 V	Positive input signal
	82	+1.3 V		0 - 200	0 - 2 V	Negative input signal
IPRE	96	-60 µA	400 nA	0 - 255	0 - -100 µA	
VPRE	1E	300 mV	10 mV	0 - 200	0 - 2 V	Value against Pile-up
IMUX	3E	-25 µA	400 nA	0 - 255	0 - -100 µA	
IBUF	6E	+44 µA	400 nA	0 - 255	0 - 100 µA	
VBUF	XX	XX	10 mV	0 - 200	0 - 2 V	No More Used
IREF	00,01,02,03	1 µA				Nominal. Value
	04	-15%				
	05	-7.5%				
	06	+7.5 %				
	07	+15 %				

The internal current reference source is adjustable around its nominal value from –15% up to +15% via REF sub-register.

BIAS_DAC format

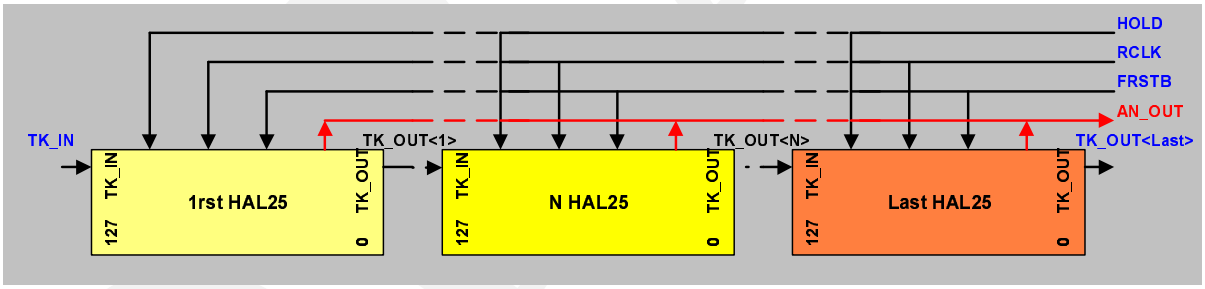
71 (MSB)								0 (LSB)
ISHCON	ISHA	VSHA	IPRE	VPRE	IMUX	IBUF	VBUF	IREF

PULSE_DAC has to be loaded only when using the Test Pulse Generator. The following table gives the hexadecimal code to set in PULSE_DAC to obtain a 10 MIPS equivalent test pulse.

Name	Code Hexa	Value	Dac Resol	Dac Range	Out Range	Notes
PULSE_DAC	64	500 µA	5 µA	0 - 255	0 - -1275 µA	10 MIPS

Readout Mode

This is a description is for the general case where many HAL25 are daisy-chained. For each chip, analogue channels are read from Channel<127> down to Channel<0>.



To perform a normal acquisition follow the protocol specified below.

1. After reset
   - HOLD, PULSE, TK_IN, RCLK, FRST must be inactive

2. Initialisation via JTAG has to be done only once
   - Set BIAS_DAC register with nominal values
   - Set TOKEN_ENA register to 1
   - Set JTAG controller in Test-Logic-Reset state

3. Parallel Acquisition
   - Upon Trigger, set and maintain HOLD active after a shaping time delay of 1.4 µS to 2.2 µS

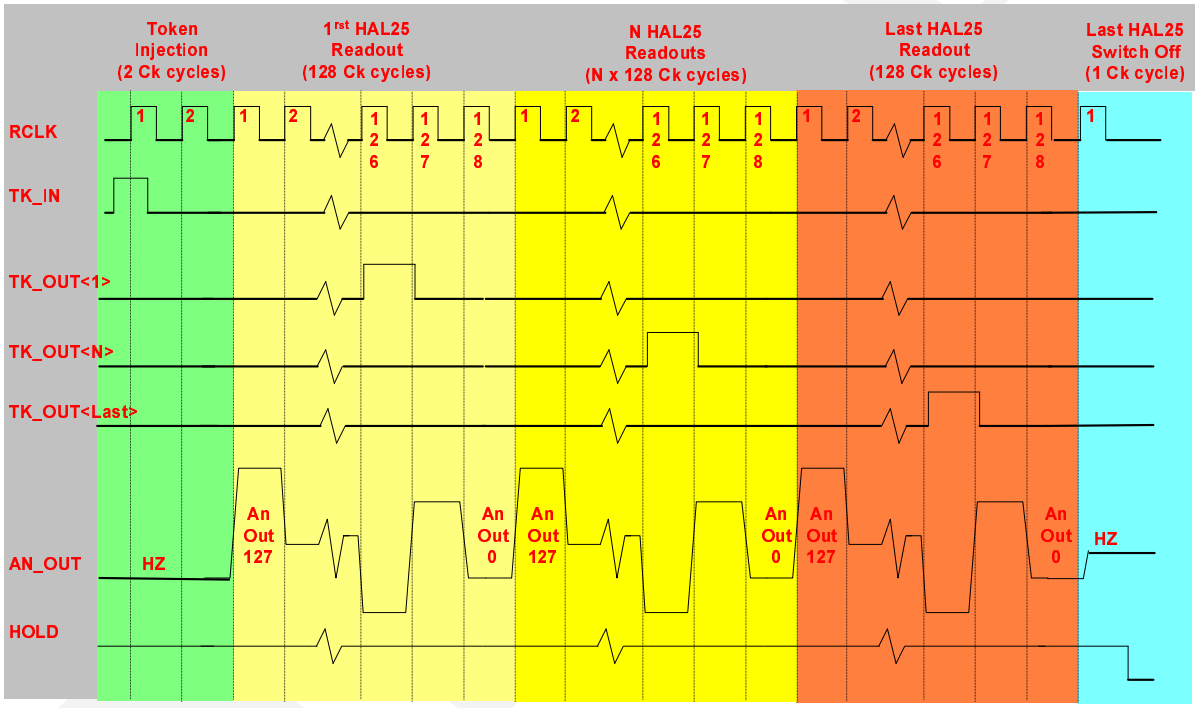
4. Serial Readout

This can be separated in 3 phases, see on the following chronogram.

1. Token Injection in the first chip
   - Sample TK_IN pulse on first RCLK. The token will shift trough the chips and active them each one after the other
   - Generate a second RCLK cycle.
     AN_OUT remains in High Z
2. HAL25 Chips Readout
   - Generate N * 128 RCLK cycles. N is the number of the daisy-chained HAL25 chips.
     Upon RCLK cycle #1, the AN_OUT output of the first chip turns active with the value of channel<127>. The AN_OUT outputs of the other chips remain in high impedance.
     Upon RCLK cycle #126, TK_OUT appears, ready to be sampled by the next HAL25.
     Upon RCLK cycle #128, the value of channel<0> appears.
     Upon RCLK cycle #129, the first chip turns in high impedance and the second turns active with channel<127> value.
3. Last Chip Switch Off
   - Generate an extra RCLK cycle.
     Last chip AN_OUT returns in High Z.
   - Release HOLD

Remark: Step 2, i.e. Chips Readout, can be aborted at any time:

- Stop cycling RCLK
- Send a FRSTB pulse
  AN_OUT returns in High Z
- Release HOLD



	Parameter	Typical Value	Notes
INIT	PWRSTB Pulse Width	5 µS	Active Low, Asynchronous Power on Reset
ACQUISITION	HOLD Delay	1.4 µS to 2.2 µS	Delay from Trigger. Depends from Shaping Time.
	HOLD Pulse Width	Active High	Until End of Readout Phase
	HOLD Dead Time	10 µS	
RE	RCLK Frequency	10 MHz	Readout Clock
	RCLK Duty Cycle	50%	Active on Rising Edge
	TK_IN Setup Time	> 20 nS, <40 nS	Active High

ADOUT	TK_IN Pulse Width	50 nS	
	AN_OUT Settling Time	50 nS	After RCLK Rising Edge
	TK_OUT Time Delay	10 nS	After RCLK Rising Edge
	FRSTB Pulse Width	100 nS	Active Low, Fast Asynchronous Reset

Pulse Test Mode

Pulse Test mode allows the user to test the analogue channels of the chip by sending a Dirac pulse with the pulse generator via the PULSE signal. This emulates the charge generated into the silicon strip detector. Positive and negative Dirac pulses are generated respectively on the rising and falling edge of PULSE.

To perform Pulse Test Mode follows the protocol below

1. After reset
   - HOLD, PULSE, TK_IN, RCLK, FRST must be inactive

2. General settings via JTAG, has to be done only once
   - Set BIAS_DAC register with nominal values
   - Set TOKEN_ENA register to 1

3. Pulse Generator setting
   - Set PULSE_DAC register with the desired current level
   - Set PULSE_REG with the desired channel selection pattern
   - Set JTAG controller in Run-Test-Idle state

4. Parallel Acquisition
   - Generate a rising or falling PULSE signal
   - Sample it by setting HOLD active after a shaping time delay of 1.4 µS to 2.2 µS

5. Serial Readout
   - To perform like in Readout Mode step 4

Pulse generator is enabled until JTAG state machine goes in Test-Logic-Reset state.

Transparent Mode

Transparent mode allows the user to check a single analogue channel among the 128. One can inject a signal and see on an oscilloscope the resulting output signal. The signal can be an external source connected to the input or the Pulse Generator configured as specified before. To set the chip in Transparent Mode follow the protocol below.

1. After reset
   - HOLD, PULSE, TK_IN, RCLK, FRST must be inactive

2. General settings via JTAG, has to be done only once
   - Set BIAS_DAC register with nominal values

3. Pulse Generator setting
   - Set PULSE_DAC register with the desired current level
   - Set PULSE_REG with the desired channel selection pattern

4. Set channel in transparent mode
   - Set POWER_ENA to 0
   - Set READ_REG register
   - Set POWER_ENA to 1
   - Set JTAG controller in Run-Test-Idle state

5. Generate a rising or falling PULSE signal

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After the test READ-REG register must be cleared. This can done by loading it with zero or sending a fast clear FRSTB.

Boundary Scan Test Mode

All the LVDS signals used for the readout of the circuit can be tested and set via BSR. One can perform a complete readout with token injection and readout clock activation.

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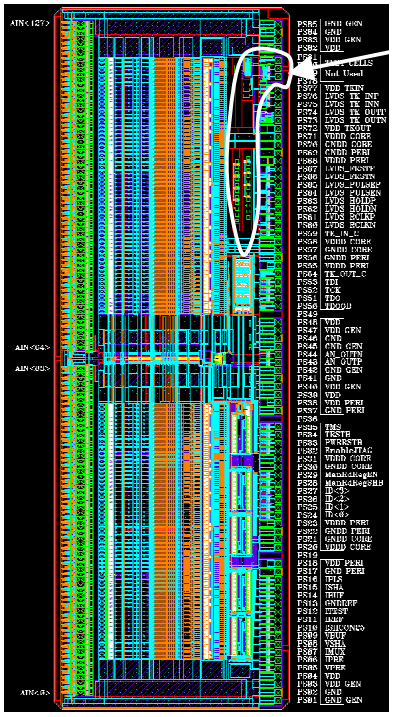
Physical Size and Pad Layout



Remark: This prototype contains an extra test structure with its own pads. They are not considered in this document.

HAL25 chip size 3650 x 10900 square microns. It is fabricated on a 0.25 µm, 3-layer metal process. The wafers are 8-inch type. The final size of the prototype submitted to the MPW4 (2001/Q1) run should not exceed 4mm X 11mm after cut. The chip should be aligned on its right hand side in the reticule. All chip coordinates are referred to its 3 butterflies. The circuit is symmetrical to the X axe.

Front End Pads

The 128 analogue inputs are grouped in 2 sections of 64 pads. They are numbered from AIN<127> down to AIN<0>. They correspond respectively to the analogue channel 127 placed on the top and to the analogue channel 0 placed at the bottom of the circuit. The 2 groups of pads are placed symmetrically to X axe. Each pad has a passivation opening size of 120 X 63 µm and has a pitch of 80 µm and contains protection diodes to VSS and VDD.

Pad	Name		Type	Value	Function
127	AIN<127>	Ana. Input	-	-	Diode Protection
...	...	...	-	-	Diode Protection
0	AIN<0>	Ana. Input	-	-	Diode Protection

Back End Pads

The 78 pads of the back-end side can be logically grouped in 4 groups:

- Power Supplies
- Readout
- Control
- Test

Each pad has a passivation opening size of 95 X 95 µm. They are placed symmetrically to the X axe with a pitch of 125 µm.
In HAL25_V2, VDD_TKOUT and VDD_TKIN pads have replaced pad VDD_TK. In order to take in account empty pad positions, pad slot numbers has replaced pad numbers. There is 85 pad slots.

Power Supply Pads

The circuit is supplied with 2.5 V. Many power pads are used in this chip. The reason is the height of HAL25 and the use of separated power for

- Analogue Block — VDD, GND pads
- Digital Block — VDDD CORE, GNDD CORE pads
- Test Pulse Generator — VDD GEN, GND GEN pads
- Digital Pads — VDDD PERI, GNDD PERI pads
- Analogue Pads — VDD PERI, GND PERI
- VDD TKIN — If connected to VDD, the pad LVDS_TK_IN is supplied and selected. If not, signal TK_IN_C is selected.
- VDD TKOUT — If connected to VDD, the pad LVDS_TK_OUT is supplied. TK_OUT_C is always selected.

The following table gives the list of the power pads. Pads listed on the same line are interconnected by metal line inside the chip.

Pad Slots	Name	Value	Function
PS84, PS46, PS41, PS02	GND	GND	Supplies for the 128 Channels, Output Buffer, and Bias. GND bias the silicon substrate of the chip. Note1.
PS82, PS48, PS39, PS04	VDD	+2.5 V	
PS71, PS58	VDDD CORE	+2.5 V	Supplies for the JTAG controller and the digital part of the analogue Mux. from Channel<127:64>. Note2
PS70, PS57	GNDD CORE	GND	
PS31, PS20	VDDD CORE	+2.5 V	Supplies for the DAC registers and the digital part of the analogue Mux. from Channel<63:0>. Note2
PS30, PS21	GNDD CORE	GND	
PS85, PS45, PS42, PS01	GND GEN	GND	Supplies of the Test Pulse Generator. Note1
PS83, PS47, PS40, PS03	VDD GEN	+2.5 V	
PS69, PS56	GNDD PERI	GND	Supplies for digital IO pads i.e. buffers and protection diodes from #67to #59 and #54 to #50. Provides also ground to LVDS_TK_x pads. Note2.
PS68, PS55	VDDD PERI	+2.5 V	
PS38	VDD PERI	+2.5 V	Supplies for analogues pads #44, #43 i.e. protection diodes. Note3
PS37	GND PERI	GND	
PS23	VDDD PERI	+2.5 V	Supplies for digital IO pads i.e. buffers and protection diodes from #35 to #32 and from #29 to #24. Note4
PS22	GNDD PERI	GND	
PS18	VDD PERI	+2.5 V	Supplies for Analogues pads #16 to #5 i.e. protection diodes. Note3
PS17	GND PERI	GND	
PS77	VDD TKIN	+2.5 V	Supplies LVDS_TK_IN pad. Note5
PS72	VDD TKOUT	+2.5 V	Supplies LVDS_TK_OUT pad. Note6

Notes:

1. If there is an unconnected pin, a performance degradation of the specified parts may be observed.
2. If there is an unconnected pin, the specified parts may have unknown behaviour.
3. If there is an unconnected pin, there will be no ESD protection but the functionality of the chip will be maintained.
4. If there is an unconnected pin, the chip cannot be operated i.e. Reset and TMS signals are not operational.
5. If VDD_TKIN is unconnected, LVDS_TK_IN is disabled. The chip can be operated via the pad TK_IN_C.
6. If VDD_TKOUT is unconnected, LVDS_TK_OUT is disabled. The chip can be operated via the pad TK_OUT_C.

Readout Pads

PS76	LVDS_TK_INP	Dig. Input	LVDS	-	Positive Token Input	Powered by VDD_TK
PS75	LVDS_TK_INN	Dig. Input	LVDS	-	Negative Token Input	No internal load
PS74	LVDS_TK_OUTP	Dig. Output	LVDS	-	Positive Token Output	Powered by VDD_TK
PS73	LVDS_TK_OUTN	Dig. Output	LVDS	-	Negative Token Output	
PS67	LVDS_FRSTP	Dig. Input	LVDS	-	Positive Fast Reset Input	No internal load
PS66	LVDS_FRSTN	Dig. Input	LVDS	-	Negative Fast Reset Input	
PS65	LVDS_PULSEP	Dig. input	LVDS	-	Positive Test Pulse Input	No internal load
PS64	LVDS_PULSEN	Dig. Input	LVDS	-	Negative Test Pulse Input	
PS63	LVDS_HOLDP	Dig. Input	LVDS	-	Positive Hold Input	No internal load
PS62	LVDS_HOLDN	Dig. input	LVDS	-	Negative Hold Input	
PS61	LVDS_RCLKP	Dig. Input	LVDS	-	Positive Clock Input	No internal load
PS60	LVDS_RCLKN	Dig. input	LVDS	-	Negative Clock Input	
PS59	TK_IN_C	Dig. input	Hyst.- PD	0/2.5 V	Cmos Token Input	active high
PS54	TK_OUT_C	Dig. Output	8 mA	0/2.5 V	Cmos Token Output	

Control Pads

PS53	TDI	Dig. Input	Hysteresis Pull Up	0/2.5 V	JTAG Data Input	Active high
PS52	TCK	Dig. Input	Hyst.- PU	0/2.5 V	JTAG Clock Input	Active high
PS51	TDO	Dig. Output	8mA - 3ST	0/2.5 V	JTAG Data Output	Active high
PS50	TDOOB	Dig. Output	8mA	0/2.5 V	JTAG Data Output	Active high
PS35	TMS	Dig. Input	Hyst.- PU	0/2.5 V	JTAG Control Input	Active high
PS34	TRSTB	Dig. Input	Hyst.- PU	0/2.5 V	JTAG Reset Input	Active low
PS33	PWRRSTB	Dig. Input	Hyst.- PU	0/2.5 V	Power on Reset Input	Active low
PS27	ID<3>	Dig. Input	Hyst.- PU	0/2.5 V	Chip ID Msb Input	Active high
PS26	ID<2>	Dig. Input	Hyst.- PU	0/2.5 V	Chip ID Input	Active high
PS25	ID<1>	Dig. Input	Hyst.- PU	0/2.5 V	Chip ID Input	Active high
PS24	ID<0>	Dig. Input	Hyst.- PU	0/2.5 V	Chip ID Lsb Input	Active high

Test Pads

PS32	EnableJTAG	Dig. Input	Hyst.- PU	0/2.5 V	Test Purpose Input	
PS29	ManRdRegEN	Dig. Input	Hyst.- PU	0/2.5 V	Test Purpose Input	
PS28	ManRdRegSHB	Dig. Input	Hyst.- PU	0/2.5 V	Test Purpose Input	
PS16	IPLS	Ana. IO			Test Purpose Input	Diodes Prot.
PS15	ISHA	Ana. IO			Test Purpose Input	Diodes Prot.
PS14	IBUF	Ana. IO			Test Purpose Input	Diodes Prot.
PS13	GNDREF	Power		GND	Gnd for Internal Current Reference Source IREF	
PS12	ITEST	Ana. Output		1 µA	IREF Probe	To Gnd or an ampere meter
PS11	IREF	Ana. Input			Internal Current Source test purpose only	Not to be used
PS10	ISHCON25	Ana. IO			Test Purpose	Diodes Prot.
PS09	VBUF	Ana. IO			Test Purpose	Diodes Prot.
PS08	VSHA	Ana. IO			Test Purpose	Diodes Prot.
PS07	IMUX	Ana. IO			Test Purpose	Diodes Prot.
PS06	IPRE	Ana. IO			Test Purpose	Diodes Prot.
PS05	VPRE	Ana. IO			Test Purpose	Diodes Prot.

Logic Levels

Digital Input

Digital Output

Analogue Output

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APPENDIX

Pad Definition

Front End Pads (Top to Bottom)

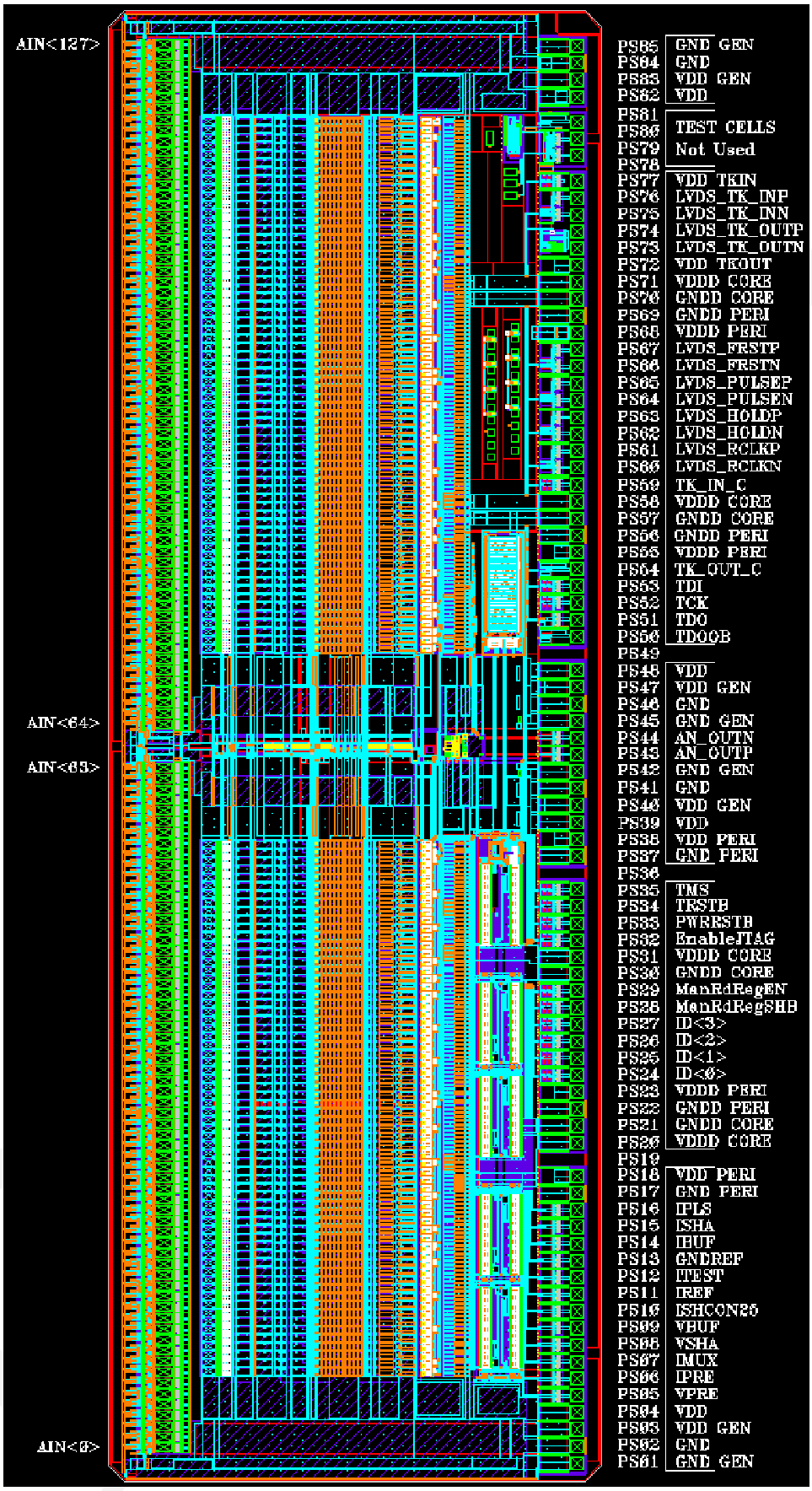
Pad	Name		Type	Value	Function
127	AIN<127>	Ana. Input	-	-	Diode Protection
126	AIN<126>	Ana. Input	-	-	Diode Protection
...	...	...	-	-	Diode Protection
0	AIN<0>	Ana. Input	-	-	Diode Protection

Back End Pad Slots (Top to Bottom)

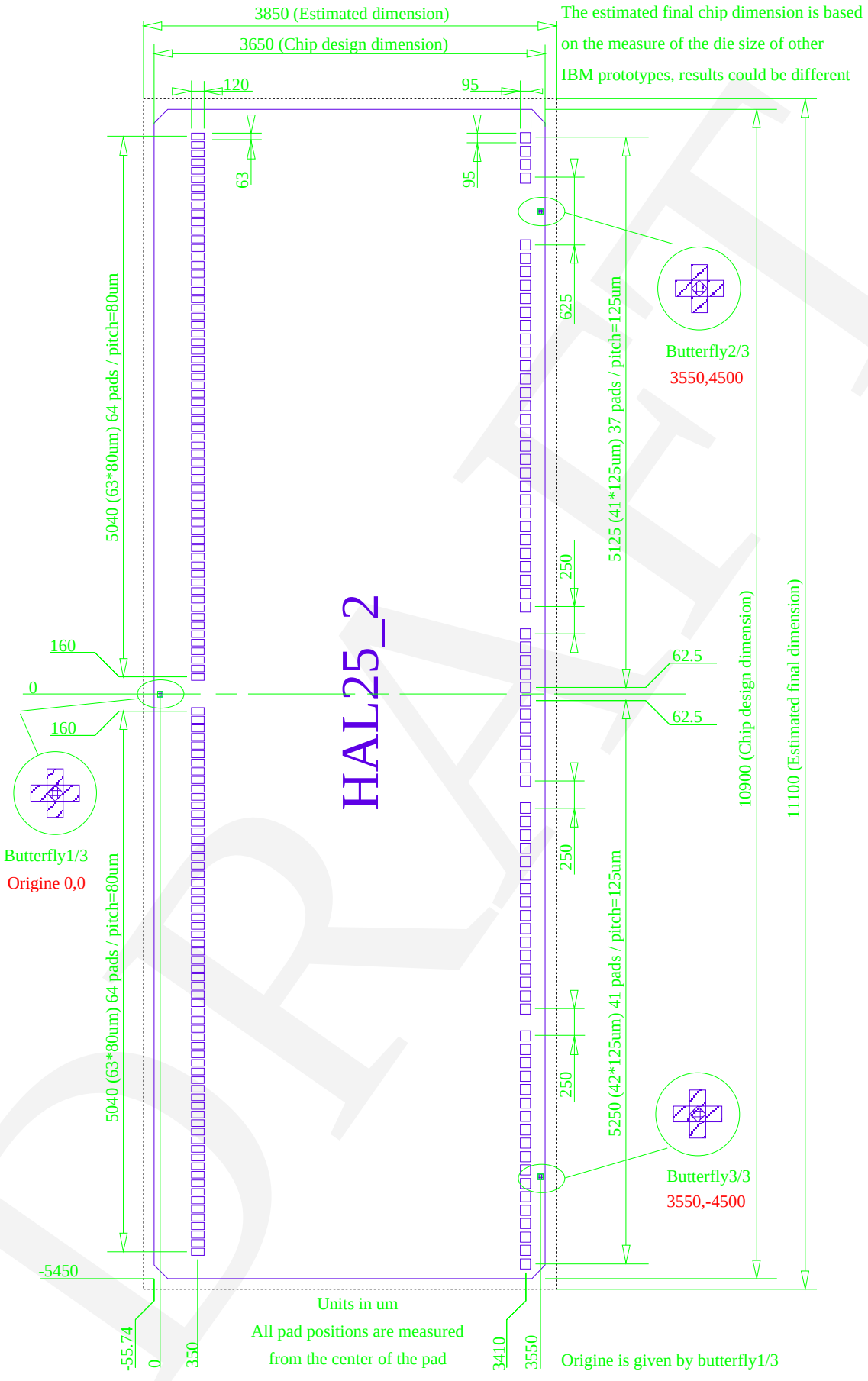
Pad	Name		Type	Value	Function	
PS85	GND GEN	Power	-	GND	Test Block Gnd	
PS84	GND	Power	-	GND	Analogue Gnd	
PS83	VDD GEN	Power	-	+2.5 V	Test Block Supply	
PS82	VDD	Power	-	+2.5 V	Analogue Positive Supply	
PS81		Empty				
PS80		Empty				
PS79		Empty				
PS78		Empty				
PS77	VDD TKIN	Power + Dig. Input	Hysteresis Pull-down	+2.5 V	Digital Positive Supply	LVDS_TK_IN pad supply
PS76	LVDS_TK_INP	Dig. Input	LVDS	-	Positive Token Input	Powered by VDD_TKIN
PS75	LVDS_TK_INN	Dig. Input	LVDS	-	Negative Token Input	No internal load
PS74	LVDS_TK_OUTP	Dig. Output	LVDS	-	Positive Token Output	Powered by VDD_TKOUT
PS73	LVDS_TK_OUTN	Dig. Output	LVDS	-	Negative Token Output	
PS72	VDD TKOUT	Power		+2.5 V	Digital Positive Supply	LVDS_TK_OUT pad supply
PS71	VDDD CORE	Power	-	+2.5 V	Digital Positive Supply	
PS70	GNDD CORE	Power	-	GND	Digital Gnd	
PS69	GNDD PERI	Power	-	GND	Digital Gnd	
PS68	VDDD PERI	Power	-	+2.5 V	Digital Positive Supply	
PS67	LVDS_FRSTP	Dig. Input	LVDS	-	Positive Fast Reset Input	No internal load
PS66	LVDS_FRSTN	Dig. Input	LVDS	-	Negative Fast Reset Input	
PS65	LVDS_PULSEP	Dig. input	LVDS	-	Positive Test Pulse Input	No internal load
PS64	LVDS_PULSEN	Dig. Input	LVDS	-	Negative Test Pulse Input	
PS63	LVDS_HOLDP	Dig. Input	LVDS	-	Positive Hold Input	No internal load
PS62	LVDS_HOLDN	Dig. input	LVDS	-	Negative Hold Input	
PS61	LVDS_RCLKP	Dig. Input	LVDS	-	Positive Clock Input	No internal load
PS60	LVDS_RCLKN	Dig. input	LVDS	-	Negative Clock Input	
PS59	TK_IN_C	Dig. input	Hyst.- PD	0/2.5 V	Cmos Token Input	active high
PS58	VDDD CORE	Power	-	+2.5 V	Digital Positive Supply	
PS57	GNDD CORE	Power	-	GND	Digital Gnd	
PS56	GNDD PERI	Power	-	GND	Digital Gnd	
PS55	VDDD PERI	Power	-	+2.5 V	Digital Positive Supply	
PS54	TK_OUT_C	Dig. Output	8 mA	0/2.5 V	Cmos Token Output	
PS53	TDI	Dig. Input	Hysteresis Pull Up	0/2.5 V	JTAG Data Input	Active high
PS52	TCK	Dig. Input	Hyst.- PU	0/2.5 V	JTAG Clock Input	Active high

PS51	TDO	Dig. Output	8mA-3ST	0/2.5 V	JTAG Data Output	Active high
PS50	TDOOB	Dig. Output	8mA	0/2.5 V	JTAG Data Output	Active high
PS49		Empty				
PS48	VDD	Power	-	+2.5 V	Analogue Positive Supply	
PS47	VDD GEN	Power	-	+2.5 V	Test Block Positive Supply	
PS46	GND	Power	-	GND	Analogue Gnd	
PS45	GND GEN	Power	-	GND	Test Block Gnd	
PS44	AN_OUTN	Ana. Output	-	-	Analogue Data Output	Diodes Prot.
PS43	AN_OUTP	Ana. Output	-	-	Analogue Data Output	Diodes Prot
PS42	GND GEN	Power	-	GND	Test Block Gnd	
PS41	GND	Power	-	GND	Analogue Gnd	
PS40	VDD GEN	Power	-	+2.5 V	Test Block Positive Supply	
PS39	VDD	Power	-	+2.5 V	Analogue Positive Supply	
PS38	VDD PERI	Power	-	+2.5 V	Digital Positive Supply	
PS37	GND PERI	Power	-	GND	Digital Gnd	
PS36		Empty				
PS35	TMS	Dig. Input	Hyst.- PU	0/2.5 V	JTAG Control Input	Active high
PS34	TRSTB	Dig. Input	Hyst.- PU	0/2.5 V	JTAG Reset Input	Active low
PS33	PWRRSTB	Dig. Input	Hyst.- PU	0/2.5 V	Power on Reset Input	Active low
PS32	EnableJTAG	Dig. Input	Hyst.- PU	0/2.5 V	Test Purpose Input	
PS31	VDDD CORE	Power	-	+2.5 V	Digital Positive Supply	
PS30	GNDD CORE	Power	-	GND	Digital Gnd	
PS29	ManRdRegEN	Dig. Input	Hyst.- PU	0/2.5 V	Test Purpose Input	
PS28	ManRdRegSHB	Dig. Input	Hyst.- PU	0/2.5 V	Test Purpose Input	
PS27	ID<3>	Dig. Input	Hyst.- PU	0/2.5 V	Chip ID Msb Input	Active high
PS26	ID<2>	Dig. Input	Hyst.- PU	0/2.5 V	Chip ID Input	Active high
PS25	ID<1>	Dig. Input	Hyst.- PU	0/2.5 V	Chip ID Input	Active high
PS24	ID<0>	Dig. Input	Hyst.- PU	0/2.5 V	Chip ID Lsb Input	Active high
PS23	VDDD PERI	Power	-	+2.5 V	Digital Positive Supply	
PS22	GNDD PERI	Power	-	GND	Digital Gnd	
PS21	GNDD CORE	Power	-	GND	Digital Gnd	
PS20	VDDD CORE	Power	-	+2.5 V	Digital Positive Supply	
PS19		Empty				
PS18	VDD PERI	Power	-	+2.5 V	Digital Positive Supply	
PS17	GND PERI	Power	-	GND	Digital Gnd	
PS16	IPLS	Ana. IO			Test Purpose Input	Diodes Prot.
PS15	ISHA	Ana. IO			Test Purpose Input	Diodes Prot.
PS14	IBUF	Ana. IO			Test Purpose Input	Diodes Prot.
PS13	GNDREF	Power		GND	Gnd for Internal Current Reference Source IREF	
PS12	ITEST	Ana. Output		1 µA	IREF Probe	To Gnd or an ampere meter
PS11	IREF	Ana. Input			Internal Current Source test purpose only	Not to be used
PS10	ISHCON25	Ana. IO			Test Purpose	Diodes Prot.
PS09	VBUF	Ana. IO			Test Purpose	Diodes Prot.
PS08	VSHA	Ana. IO			Test Purpose	Diodes Prot.
PS07	IMUX	Ana. IO			Test Purpose	Diodes Prot.
PS06	IPRE	Ana. IO			Test Purpose	Diodes Prot.
PS05	VPRE	Ana. IO			Test Purpose	Diodes Prot.
PS04	VDD	Power	-	+2.5 V	Analogue Positive Supply	
PS03	VDD GEN	Power	-	+2.5 V	Test Block Supply	
PS02	GND	Power	-	GND	Analogue Gnd	
PS01	GND GEN	Power	-	GND	Test Block Gnd	

Physical Layout



Physical Size



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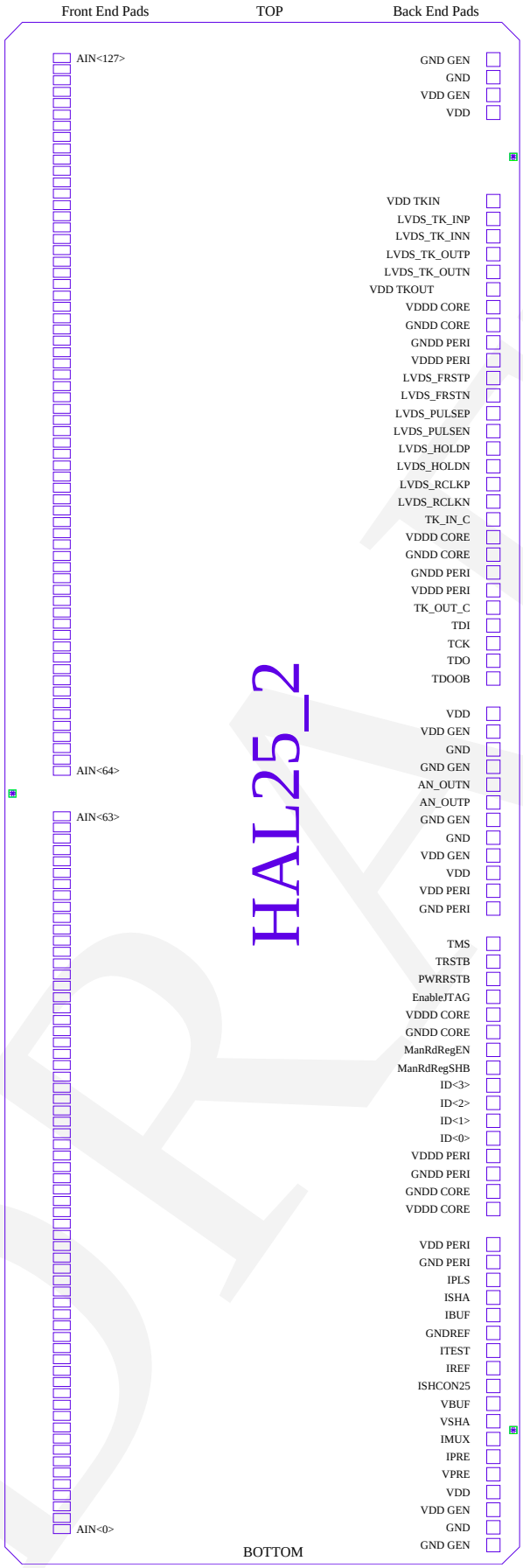
Pad Layout



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Pad Coordinates

Chip design dimension from butterfly origin, unit μm

	X1	Y1	X2	Y2
	-55.74	-5450	3594.26	5450

Absolute chip design dimension, unit in μm

	X	Y
	3650	10900

Input Pads: Size H=63μm, L=120μum, Y Pitch=80μm

Coordinates of Passivation Opening in nm						Unit in micrometers					
Pin #	X1	Y1	X2	Y2		X Center	Y Center	X Pitch	Y Pitch	Length	High
127	345740	5168500	465740	5231500		405.74	5200			120	63
126	345740	5088500	465740	5151500		405.74	5120	0	80	120	63
125	345740	5008500	465740	5071500		405.74	5040	0	80	120	63
124	345740	4928500	465740	4991500		405.74	4960	0	80	120	63
123	345740	4848500	465740	4911500		405.74	4880	0	80	120	63
122	345740	4768500	465740	4831500		405.74	4800	0	80	120	63
121	345740	4688500	465740	4751500		405.74	4720	0	80	120	63
120	345740	4608500	465740	4671500		405.74	4640	0	80	120	63
119	345740	4528500	465740	4591500		405.74	4560	0	80	120	63
118	345740	4448500	465740	4511500		405.74	4480	0	80	120	63
117	345740	4368500	465740	4431500		405.74	4400	0	80	120	63
116	345740	4288500	465740	4351500		405.74	4320	0	80	120	63
115	345740	4208500	465740	4271500		405.74	4240	0	80	120	63
114	345740	4128500	465740	4191500		405.74	4160	0	80	120	63
113	345740	4048500	465740	4111500		405.74	4080	0	80	120	63
112	345740	3968500	465740	4031500		405.74	4000	0	80	120	63
111	345740	3888500	465740	3951500		405.74	3920	0	80	120	63
110	345740	3808500	465740	3871500		405.74	3840	0	80	120	63
109	345740	3728500	465740	3791500		405.74	3760	0	80	120	63
108	345740	3648500	465740	3711500		405.74	3680	0	80	120	63
107	345740	3568500	465740	3631500		405.74	3600	0	80	120	63
106	345740	3488500	465740	3551500		405.74	3520	0	80	120	63
105	345740	3408500	465740	3471500		405.74	3440	0	80	120	63
104	345740	3328500	465740	3391500		405.74	3360	0	80	120	63
103	345740	3248500	465740	3311500		405.74	3280	0	80	120	63
102	345740	3168500	465740	3231500		405.74	3200	0	80	120	63
101	345740	3088500	465740	3151500		405.74	3120	0	80	120	63
100	345740	3008500	465740	3071500		405.74	3040	0	80	120	63
99	345740	2928500	465740	2991500		405.74	2960	0	80	120	63
98	345740	2848500	465740	2911500		405.74	2880	0	80	120	63
97	345740	2768500	465740	2831500		405.74	2800	0	80	120	63
96	345740	2688500	465740	2751500		405.74	2720	0	80	120	63
95	345740	2608500	465740	2671500		405.74	2640	0	80	120	63
94	345740	2528500	465740	2591500		405.74	2560	0	80	120	63
93	345740	2448500	465740	2511500		405.74	2480	0	80	120	63
92	345740	2368500	465740	2431500		405.74	2400	0	80	120	63
91	345740	2288500	465740	2351500		405.74	2320	0	80	120	63
90	345740	2208500	465740	2271500		405.74	2240	0	80	120	63
89	345740	2128500	465740	2191500		405.74	2160	0	80	120	63
88	345740	2048500	465740	2111500		405.74	2080	0	80	120	63
87	345740	1968500	465740	2031500		405.74	2000	0	80	120	63
86	345740	1888500	465740	1951500		405.74	1920	0	80	120	63
85	345740	1808500	465740	1871500		405.74	1840	0	80	120	63
84	345740	1728500	465740	1791500		405.74	1760	0	80	120	63
83	345740	1648500	465740	1711500		405.74	1680	0	80	120	63
82	345740	1568500	465740	1631500		405.74	1600	0	80	120	63
81	345740	1488500	465740	1551500		405.74	1520	0	80	120	63
80	345740	1408500	465740	1471500		405.74	1440	0	80	120	63
79	345740	1328500	465740	1391500		405.74	1360	0	80	120	63
78	345740	1248500	465740	1311500		405.74	1280	0	80	120	63
77	345740	1168500	465740	1231500		405.74	1200	0	80	120	63

76	345740	1088500	465740	1151500		405.74	1120	0	80	120	63
75	345740	1008500	465740	1071500		405.74	1040	0	80	120	63
74	345740	928500	465740	991500		405.74	960	0	80	120	63
73	345740	848500	465740	911500		405.74	880	0	80	120	63
72	345740	768500	465740	831500		405.74	800	0	80	120	63
71	345740	688500	465740	751500		405.74	720	0	80	120	63
70	345740	608500	465740	671500		405.74	640	0	80	120	63
69	345740	528500	465740	591500		405.74	560	0	80	120	63
68	345740	448500	465740	511500		405.74	480	0	80	120	63
67	345740	368500	465740	431500		405.74	400	0	80	120	63
66	345740	288500	465740	351500		405.74	320	0	80	120	63
65	345740	208500	465740	271500		405.74	240	0	80	120	63
64	345740	128500	465740	191500		405.74	160	0	80	120	63
63	345740	-191500	465740	-128500		405.74	-160	0	320	120	63
62	345740	-271500	465740	-208500		405.74	-240	0	80	120	63
61	345740	-351500	465740	-288500		405.74	-320	0	80	120	63
60	345740	-431500	465740	-368500		405.74	-400	0	80	120	63
59	345740	-511500	465740	-448500		405.74	-480	0	80	120	63
58	345740	-591500	465740	-528500		405.74	-560	0	80	120	63
57	345740	-671500	465740	-608500		405.74	-640	0	80	120	63
56	345740	-751500	465740	-688500		405.74	-720	0	80	120	63
55	345740	-831500	465740	-768500		405.74	-800	0	80	120	63
54	345740	-911500	465740	-848500		405.74	-880	0	80	120	63
53	345740	-991500	465740	-928500		405.74	-960	0	80	120	63
52	345740	-1071500	465740	-1008500		405.74	-1040	0	80	120	63
51	345740	-1151500	465740	-1088500		405.74	-1120	0	80	120	63
50	345740	-1231500	465740	-1168500		405.74	-1200	0	80	120	63
49	345740	-1311500	465740	-1248500		405.74	-1280	0	80	120	63
48	345740	-1391500	465740	-1328500		405.74	-1360	0	80	120	63
47	345740	-1471500	465740	-1408500		405.74	-1440	0	80	120	63
46	345740	-1551500	465740	-1488500		405.74	-1520	0	80	120	63
45	345740	-1631500	465740	-1568500		405.74	-1600	0	80	120	63
44	345740	-1711500	465740	-1648500		405.74	-1680	0	80	120	63
43	345740	-1791500	465740	-1728500		405.74	-1760	0	80	120	63
42	345740	-1871500	465740	-1808500		405.74	-1840	0	80	120	63
41	345740	-1951500	465740	-1888500		405.74	-1920	0	80	120	63
40	345740	-2031500	465740	-1968500		405.74	-2000	0	80	120	63
39	345740	-2111500	465740	-2048500		405.74	-2080	0	80	120	63
38	345740	-2191500	465740	-2128500		405.74	-2160	0	80	120	63
37	345740	-2271500	465740	-2208500		405.74	-2240	0	80	120	63
36	345740	-2351500	465740	-2288500		405.74	-2320	0	80	120	63
35	345740	-2431500	465740	-2368500		405.74	-2400	0	80	120	63
34	345740	-2511500	465740	-2448500		405.74	-2480	0	80	120	63
33	345740	-2591500	465740	-2528500		405.74	-2560	0	80	120	63
32	345740	-2671500	465740	-2608500		405.74	-2640	0	80	120	63
31	345740	-2751500	465740	-2688500		405.74	-2720	0	80	120	63
30	345740	-2831500	465740	-2768500		405.74	-2800	0	80	120	63
29	345740	-2911500	465740	-2848500		405.74	-2880	0	80	120	63
28	345740	-2991500	465740	-2928500		405.74	-2960	0	80	120	63
27	345740	-3071500	465740	-3008500		405.74	-3040	0	80	120	63
26	345740	-3151500	465740	-3088500		405.74	-3120	0	80	120	63
25	345740	-3231500	465740	-3168500		405.74	-3200	0	80	120	63
24	345740	-3311500	465740	-3248500		405.74	-3280	0	80	120	63
23	345740	-3391500	465740	-3328500		405.74	-3360	0	80	120	63
22	345740	-3471500	465740	-3408500		405.74	-3440	0	80	120	63
21	345740	-3551500	465740	-3488500		405.74	-3520	0	80	120	63
20	345740	-3631500	465740	-3568500		405.74	-3600	0	80	120	63
19	345740	-3711500	465740	-3648500		405.74	-3680	0	80	120	63
18	345740	-3791500	465740	-3728500		405.74	-3760	0	80	120	63
17	345740	-3871500	465740	-3808500		405.74	-3840	0	80	120	63
16	345740	-3951500	465740	-3888500		405.74	-3920	0	80	120	63
15	345740	-4031500	465740	-3968500		405.74	-4000	0	80	120	63

14	345740	-4111500	465740	-4048500		405.74	-4080	0	80	120	63
13	345740	-4191500	465740	-4128500		405.74	-4160	0	80	120	63
12	345740	-4271500	465740	-4208500		405.74	-4240	0	80	120	63
11	345740	-4351500	465740	-4288500		405.74	-4320	0	80	120	63
10	345740	-4431500	465740	-4368500		405.74	-4400	0	80	120	63
9	345740	-4511500	465740	-4448500		405.74	-4480	0	80	120	63
8	345740	-4591500	465740	-4528500		405.74	-4560	0	80	120	63
7	345740	-4671500	465740	-4608500		405.74	-4640	0	80	120	63
6	345740	-4751500	465740	-4688500		405.74	-4720	0	80	120	63
5	345740	-4831500	465740	-4768500		405.74	-4800	0	80	120	63
4	345740	-4911500	465740	-4848500		405.74	-4880	0	80	120	63
3	345740	-4991500	465740	-4928500		405.74	-4960	0	80	120	63
2	345740	-5071500	465740	-5008500		405.74	-5040	0	80	120	63
1	345740	-5151500	465740	-5088500		405.74	-5120	0	80	120	63
0	345740	-5231500	465740	-5168500		405.74	-5200	0	80	120	63
Pin #	X1	Y1	X2	Y2		X Center	Y Center	X Pitch	Y Pitch	Length	High

Output Pads: Size H=95µm, L=95µm, Y Pitch=modulo 125µm

Coordinates of Passivation Opening in nm						Unit in micrometers					
Pad Slot #	X1	Y1	X2	Y2		X Center	Y Center	X Pitch	YPitch	Length	High
PS 85	3418240	5140000	3513240	5235000		3465.74	5187.5			95	95
PS 84	3418240	5015000	3513240	5110000		3465.74	5062.5	0	125	95	95
PS 83	3418240	4890000	3513240	4985000		3465.74	4937.5	0	125	95	95
PS 82	3418240	4765000	3513240	4860000		3465.74	4812.5	0	125	95	95
PS 81											
PS 80		**No Pads**									
PS 79											
PS 78											
PS 77	3418240	4140000	3513240	4235000		3465.74	4187.5	0	625	95	95
PS 76	3418240	4015000	3513240	4110000		3465.74	4062.5	0	125	95	95
PS 75	3418240	3890000	3513240	3985000		3465.74	3937.5	0	125	95	95
PS 74	3418240	3765000	3513240	3860000		3465.74	3812.5	0	125	95	95
PS 73	3418240	3640000	3513240	3735000		3465.74	3687.5	0	125	95	95
PS 72	3418240	3515000	3513240	3610000		3465.74	3562.5	0	125	95	95
PS 71	3418240	3390000	3513240	3485000		3465.74	3437.5	0	125	95	95
PS 70	3418240	3265000	3513240	3360000		3465.74	3312.5	0	125	95	95
PS 69	3418240	3140000	3513240	3235000		3465.74	3187.5	0	125	95	95
PS 68	3418240	3015000	3513240	3110000		3465.74	3062.5	0	125	95	95
PS 67	3418240	2890000	3513240	2985000		3465.74	2937.5	0	125	95	95
PS 66	3418240	2765000	3513240	2860000		3465.74	2812.5	0	125	95	95
PS 65	3418240	2640000	3513240	2735000		3465.74	2687.5	0	125	95	95
PS 64	3418240	2515000	3513240	2610000		3465.74	2562.5	0	125	95	95
PS 63	3418240	2390000	3513240	2485000		3465.74	2437.5	0	125	95	95
PS 62	3418240	2265000	3513240	2360000		3465.74	2312.5	0	125	95	95
PS 61	3418240	2140000	3513240	2235000		3465.74	2187.5	0	125	95	95
PS 60	3418240	2015000	3513240	2110000		3465.74	2062.5	0	125	95	95
PS 59	3418240	1890000	3513240	1985000		3465.74	1937.5	0	125	95	95
PS 58	3418240	1765000	3513240	1860000		3465.74	1812.5	0	125	95	95
PS 57	3418240	1640000	3513240	1735000		3465.74	1687.5	0	125	95	95
PS 56	3418240	1515000	3513240	1610000		3465.74	1562.5	0	125	95	95
PS 55	3418240	1390000	3513240	1485000		3465.74	1437.5	0	125	95	95
PS 54	3418240	1265000	3513240	1360000		3465.74	1312.5	0	125	95	95
PS 53	3418240	1140000	3513240	1235000		3465.74	1187.5	0	125	95	95
PS 52	3418240	1015000	3513240	1110000		3465.74	1062.5	0	125	95	95
PS 51	3418240	890000	3513240	985000		3465.74	937.5	0	125	95	95
PS 50	3418240	765000	3513240	860000		3465.74	812.5	0	125	95	95
PS 49		**No Pads**									
PS 48	3418240	515000	3513240	610000		3465.74	562.5	0	250	95	95
PS 47	3418240	390000	3513240	485000		3465.74	437.5	0	125	95	95
PS 46	3418240	265000	3513240	360000		3465.74	312.5	0	125	95	95
PS 45	3418240	140000	3513240	235000		3465.74	187.5	0	125	95	95

PS	44	3418240	15000	3513240	110000		3465.74	62.5	0	125	95	95
PS	43	3418240	-110000	3513240	-15000		3465.74	-62.5	0	125	95	95
PS	42	3418240	-235000	3513240	-140000		3465.74	-187.5	0	125	95	95
PS	41	3418240	-360000	3513240	-265000		3465.74	-312.5	0	125	95	95
PS	40	3418240	-485000	3513240	-390000		3465.74	-437.5	0	125	95	95
PS	39	3418240	-610000	3513240	-515000		3465.74	-562.5	0	125	95	95
PS	38	3418240	-735000	3513240	-640000		3465.74	-687.5	0	125	95	95
PS	37	3418240	-860000	3513240	-765000		3465.74	-812.5	0	125	95	95
PS	36	**No Pads**										
PS	35	3418240	-1110000	3513240	-1015000		3465.74	-1062.5	0	250	95	95
PS	34	3418240	-1235000	3513240	-1140000		3465.74	-1187.5	0	125	95	95
PS	33	3418240	-1360000	3513240	-1265000		3465.74	-1312.5	0	125	95	95
PS	32	3418240	-1485000	3513240	-1390000		3465.74	-1437.5	0	125	95	95
PS	31	3418240	-1610000	3513240	-1515000		3465.74	-1562.5	0	125	95	95
PS	30	3418240	-1735000	3513240	-1640000		3465.74	-1687.5	0	125	95	95
PS	29	3418240	-1860000	3513240	-1765000		3465.74	-1812.5	0	125	95	95
PS	28	3418240	-1985000	3513240	-1890000		3465.74	-1937.5	0	125	95	95
PS	27	3418240	-2110000	3513240	-2015000		3465.74	-2062.5	0	125	95	95
PS	26	3418240	-2235000	3513240	-2140000		3465.74	-2187.5	0	125	95	95
PS	25	3418240	-2360000	3513240	-2265000		3465.74	-2312.5	0	125	95	95
PS	24	3418240	-2485000	3513240	-2390000		3465.74	-2437.5	0	125	95	95
PS	23	3418240	-2610000	3513240	-2515000		3465.74	-2562.5	0	125	95	95
PS	22	3418240	-2735000	3513240	-2640000		3465.74	-2687.5	0	125	95	95
PS	21	3418240	-2860000	3513240	-2765000		3465.74	-2812.5	0	125	95	95
PS	20	3418240	-2985000	3513240	-2890000		3465.74	-2937.5	0	125	95	95
PS	19	**No Pads**										
PS	18	3418240	-3235000	3513240	-3140000		3465.74	-3187.5	0	250	95	95
PS	17	3418240	-3360000	3513240	-3265000		3465.74	-3312.5	0	125	95	95
PS	16	3418240	-3485000	3513240	-3390000		3465.74	-3437.5	0	125	95	95
PS	15	3418240	-3610000	3513240	-3515000		3465.74	-3562.5	0	125	95	95
PS	14	3418240	-3735000	3513240	-3640000		3465.74	-3687.5	0	125	95	95
PS	13	3418240	-3860000	3513240	-3765000		3465.74	-3812.5	0	125	95	95
PS	12	3418240	-3985000	3513240	-3890000		3465.74	-3937.5	0	125	95	95
PS	11	3418240	-4110000	3513240	-4015000		3465.74	-4062.5	0	125	95	95
PS	10	3418240	-4235000	3513240	-4140000		3465.74	-4187.5	0	125	95	95
PS	09	3418240	-4360000	3513240	-4265000		3465.74	-4312.5	0	125	95	95
PS	08	3418240	-4485000	3513240	-4390000		3465.74	-4437.5	0	125	95	95
PS	07	3418240	-4610000	3513240	-4515000		3465.74	-4562.5	0	125	95	95
PS	06	3418240	-4735000	3513240	-4640000		3465.74	-4687.5	0	125	95	95
PS	05	3418240	-4860000	3513240	-4765000		3465.74	-4812.5	0	125	95	95
PS	04	3418240	-4985000	3513240	-4890000		3465.74	-4937.5	0	125	95	95
PS	03	3418240	-5110000	3513240	-5015000		3465.74	-5062.5	0	125	95	95
PS	02	3418240	-5235000	3513240	-5140000		3465.74	-5187.5	0	125	95	95
PS	01	3418240	-5360000	3513240	-5265000		3465.74	-5312.5	0	125	95	95
Pad	Slot #	X1	Y1	X2	Y2		X Center	Y Center	X Pitch	Y Pitch	Length	High